For the JFET:

- The structure is symmetric around $y = 0$. This allows us to essentially slice the problem in half and work on just the upper half.
- t is the physical width of the n-type channel.
- N_D is the uniform doping in the channel.
- We will assume that gate diode has $N_A >> N_D$, so that we can treat the diode as being essentially one-sided
- ϕ_{bi} is the built-in potential of the reversed biased gate diode.

Using the depletion approximation, the width of the reverse-biased gate depletion layer is

$$X_n = \sqrt{\frac{2\epsilon\left(\phi_{bi} - V_{GS}\right)}{qN_D}}$$

The width of the undepleted portion of the channel is

$$t - 2X_n = t - 2\sqrt{\frac{2\epsilon\left(\phi_{bi} - V_{GS}\right)}{qN_D}}$$

The condition for pinching off the channel is when $t - 2X_n = 0$.

$$t = 2\sqrt{\frac{2\epsilon\left(\phi_{bi} - V_P\right)}{qN_D}}$$

At the pinch-off, the reverse-bias on the gate is the *pinch-off* voltage:

$$V_p = \phi_{bi} - \frac{qN_D t^2}{8\epsilon}$$

Of course, if the channel is completely pinched off, no current can flow. Therefore, the range of possible gate voltages is $V_P < V_{GS} < 0$. (Actually, the gate voltage could be made slightly positive, as long as the diode does not being too forward biased. Current flowing from the gate to the channel is not acceptable.)

The sheet concentration of the undepleted part of the channel is

$$n_s = N_D \left(t - 2X_n\right)$$

$$= N_D \left(t - 2\sqrt{\frac{2\epsilon\left(\phi_{bi} - V_{GS}\right)}{qN_D}} \right)$$

$$= N_D \left(t - 2\sqrt{\frac{2\epsilon\phi_{bi}}{qN_D}}\sqrt{1 - \frac{V_{GS}}{\phi_{bi}}} \right)$$

$$= N_D \left(t - 2X_{no}\sqrt{1 - \frac{V_{GS}}{\phi_{bi}}} \right)$$

where X_{no} is the zero-bias depletion-layer width of the gate diode.

If the channel is not pinched off, we cause drain current to flow by increasing the drain voltage, $V_{DS} > 0$. If V_{DS} is very small, the shape of the channel is approximately uniform form the source to the drain. The undeleted portion of the channel can be treated as a simple resistor,.

$$R_{DS} = \frac{\rho L}{W\left(t - 2X_n\right)}$$

$$= \frac{L}{q\mu_n N_D W\left(t - 2X_n\right)}$$

$$= \frac{L}{q\mu_n n_s W}$$

$$= \frac{\frac{L}{W}}{q\mu_n N_D\left(t - 2X_{no}\sqrt{1 - \frac{V_{GS}}{\phi_{bi}}}\right)}$$

Maximum channel width (minimum channel resistance) when $V_{GS} = 0$.

However, the increasing drain voltage *does* affect the shape of the channel. Increasing the drain voltage has the effect of increasing the reverse bias on the gate junction at the drain end, meaning that the channel is narrower and the electron sheet concentration is smaller. At the source end the undepleted width and the sheet concentration are:

$$t - 2X_n(0) = t - 2\sqrt{\frac{2\epsilon\left(\phi_{bi} - V_{GS}\right)}{qN_D}}$$

$$n_s(0) = N_D\left(t - 2X_{no}\sqrt{1 - \frac{V_{GS}}{\phi_{bi}}}\right)$$

Those quantities at the drain end are:

$$t - 2X_n(L) = t - 2\sqrt{\frac{2\epsilon\left(\phi_{bi} - V_{GS} + V_{DS}\right)}{qN_D}}$$

$$n_s(L) = N_D\left(t - 2X_{no}\sqrt{1 + \frac{V_{DS} - V_{GS}}{\phi_{bi}}}\right)$$

The electrostatic potential difference that controls of the width of the depletion layer from $\phi_{bi} - V_{GS}$ at the source to $\phi_{bi} - V_{GS} + V_{DS}$ at the drain end. If we assume that the electrostatic potential varies linearly from one end to the other (a rather big assumption), then at any point along the channel, the potential is $\phi_{bi} - V_{GS} + \phi(x)$, where $\phi(0) = 0$ at the source end and $\phi(L) = V_{DS}$ at the drain end.

The sheet concentration is then a function of ϕ as ϕ varies down the channel.

$$n_s(\phi) = N_D \left(t - 2X_{no}\sqrt{1 + \frac{\phi - V_{GS}}{\phi_{bi}}} \right)$$

Now we can invoke our generalized drain current equation from the previous lecture:

$$I_D = \frac{qW}{L} \int_0^{V_{DS}} \mu_n(\phi)\, n_s(\phi)\, d\phi$$

In the JFET case, we can assume that the mobility is constant — it will depend only on the doping level.

$$I_D = \frac{q\mu_n W}{L}\int_0^{V_{DS}} n_s(\phi)\, d\phi$$

$$= \frac{q\mu_n N_D W}{L}\int_0^{V_{DS}} \left(t - 2X_{no}\sqrt{1 + \frac{\phi - V_{GS}}{\phi_{bi}}} \right) d\phi$$

$$= \frac{q\mu_n N_D W t}{L}\int_0^{V_{DS}} \left(1 - \frac{2X_{no}}{t}\sqrt{1 + \frac{\phi - V_{GS}}{\phi_{bi}}} \right) d\phi$$

Grinding through the integration:

$$I_D = \frac{q\mu_n N_D W t}{L}\left\{ V_{DS} - \frac{4\phi_{bi}X_{no}}{3t}\left[\left(1 + \frac{V_{DS} - V_{GS}}{\phi_{bi}} \right)^{3/2} - \left(1 - \frac{V_{GS}}{\phi_{bi}} \right)^{3/2} \right] \right\}$$

Yee-ikes!! This is messy. But we now see that the drain current is a function of gate voltage *and* drain voltage, as we expect for a FET.