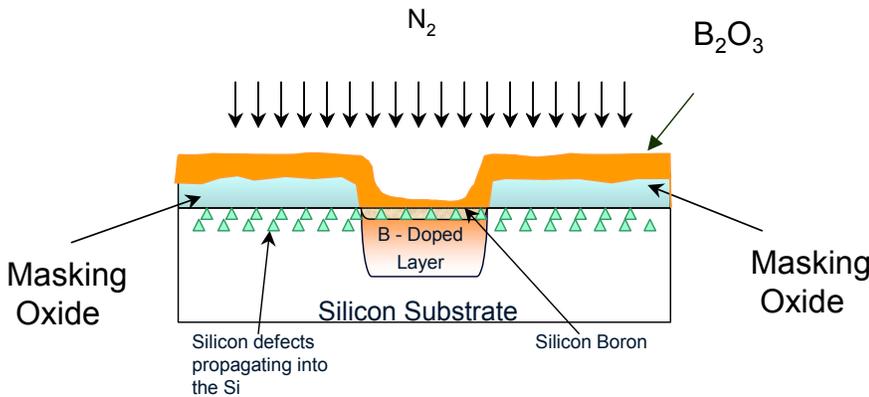


# Silicon Boron Layer (Si-B) & Low Temperature Oxidation

Depositions using PDS® Products boron nitride solid source wafers on silicon substrate develop a silicon-boron phase (boron skin). The phase is a result of excess boron reacting with the silicon surface and is typically 200 Å thick and is not effected by HF. This boron skin is the fundamental reason for the gettering properties of the BN-975.

**Figure 1. Silicon Wafer Cross Section After Boron Diffusion**

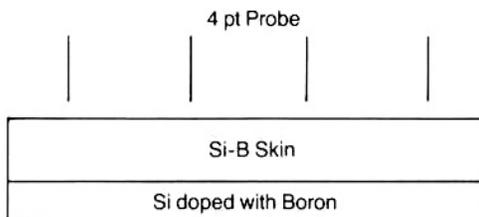


Additional diffusion processing during the IC manufacturing process mandates the removal of the boron skin. If this layer is not removed, any defects “held” within this layer will propagate deeper into the silicon substrate during subsequent thermal processing. In addition to the defect issue, the Si-B layer will act as a source of boron. The significance is higher surface concentration than expected.

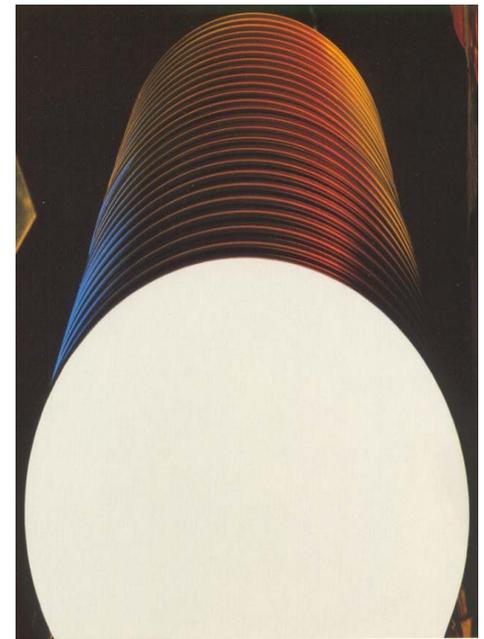
After the Si wafers are unloaded from the furnace, the excess un-reacted dopant glass is removed by a boron etch, such as 10:1 HF. Many different boron glass etches, even hot water, can be used for this purpose. After deglaze, the silicon surface is hydrophilic (i.e. wets) due to the presence of the un-etchable Si-B layer. This layer is typically 200Å thick. At this stage of the process, wetting of the silicon is acceptable, as the next stage of treatment will remove the Si-B and some Si along with the defects.

If a four point probe resistivity check is performed at this time, the sheet resistivity measurements will be lower than after the Si-B phase is removed due to the fact that the probe is measuring the lower resistivity of the Si-B layer in parallel with the diffused layer beneath it (Figure 2). Measurements at this time are valid process checks. Deglazing and probing following the low temperature oxidation will determine the amount of resistivity shift. Typically, there is a 5% to 10% resistivity shift.

**Figure 2. Si-B layer in parallel with the diffused layer.**



# Boron Nitride Grade PDS Products Technical Bulletin



## Low Temperature Oxidation

**SAINT-GOBAIN ADVANCED CERAMICS** LTO is 100% dry Oxygen at 750 °C for 20 min

**SAINT-GOBAIN ADVANCED CERAMICS** Defect control is a result of removing the defects and damage "pinned" in the Si-B layer

**SAINT-GOBAIN ADVANCED CERAMICS** LTO consumes Silicon to form SiO<sub>2</sub> converting the un-etchable Si-B to SiO<sub>2</sub> and Boron.

**SAINT-GOBAIN ADVANCED CERAMICS** Silicon damage is removed with HF etch

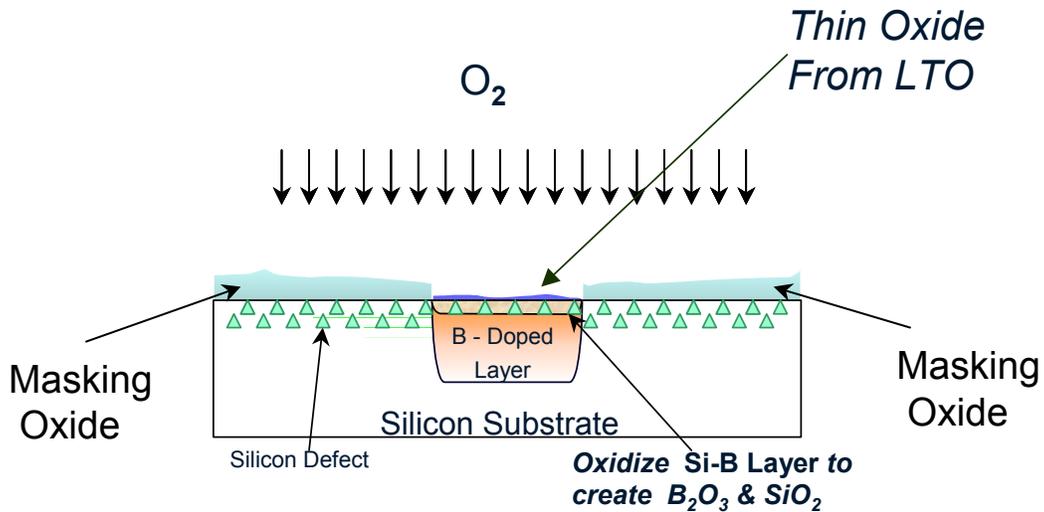
**SAINT-GOBAIN ADVANCED CERAMICS** LTO is a three-step process:

- 1) HF etch (Deglaze) after Deposition
- 2) Silicon Oxidation (LTO)
- 3) Deglaze after LTO

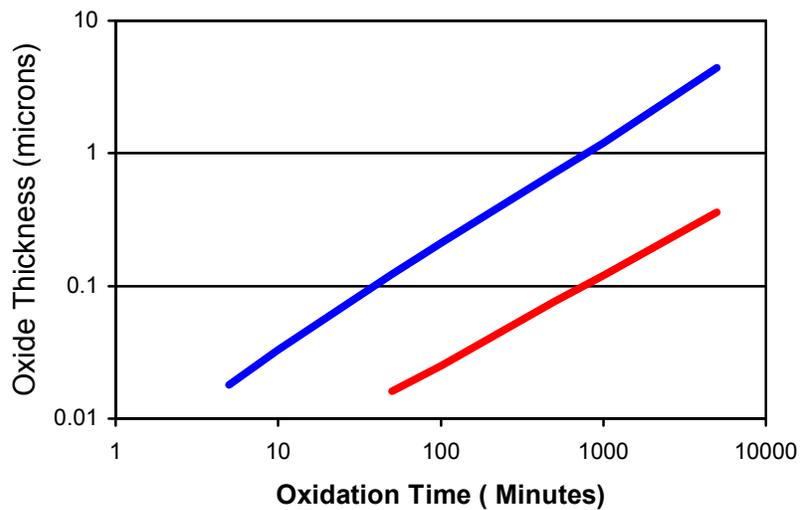
## Low Temperature Oxidation (LTO)

The function of the LTO step is to oxidize the Si-B layer and a thin layer of Si below it (Figure 3). Oxidizing this thin Si layer will immobilize most of the crystal defects in the oxide. A steam or  $O_2$  ambient (Figure 4.) is typically used to cause the rapid oxidation of the Si-B layer and its silicon interface region before harmful propagation of the defects into the silicon can occur. This allows the subsequent drive cycle to be damage free.

**Figure 3. Oxidation of Si-B and a thin layer of Si**



**Figure 4. Wet vs. Dry Silicon Oxidation Curves**

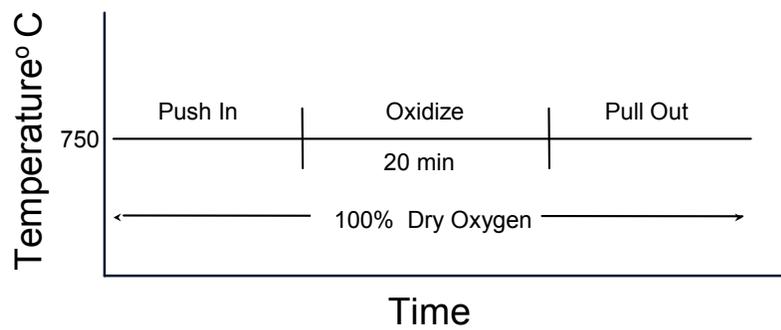


## Low Temperature Oxidation (LTO) Procedure

LTO is a three - step process:

- 1) HF etch (Deglaze) after deposition
  - 10:1 DiH<sub>2</sub>O to 49%HF - 2 minutes
  - Removes B<sub>2</sub>O<sub>3</sub> glass from the exposed silicon surface

Also removes some of the doped masking oxide
- 2) Silicon Oxidation
  - 750 °C for 20 minutes in 100% O<sub>2</sub>

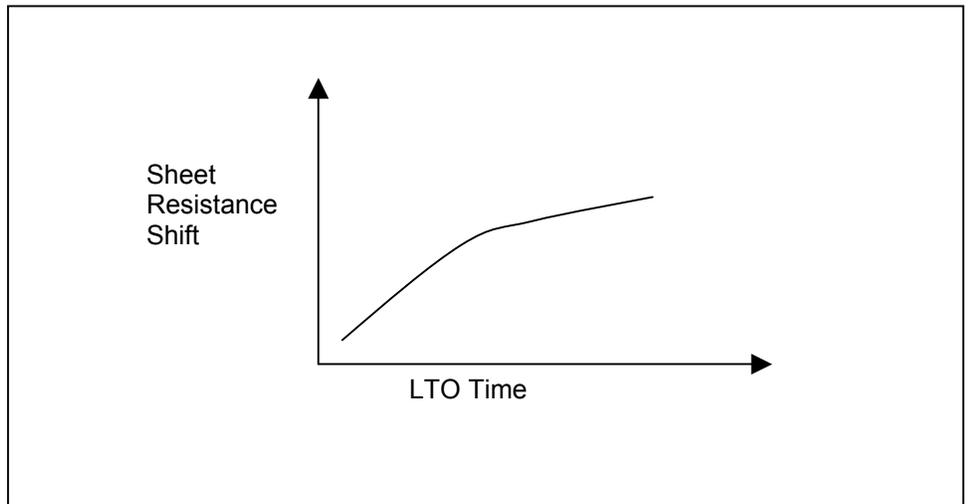


- 3) Deglaze after LTO:
  - 10:1 DiH<sub>2</sub>O to HF - 2 minutes
  - Removes the B<sub>2</sub>O<sub>3</sub> / SiO<sub>2</sub> layer created by oxidizing the Silicon Boron (Si-B) layer.
  - Removes defects "pinned" in the oxidized Si-B layer
  - Also removes some of the masking oxide

## Optimizing the LTO Process

To determine the optimum LTO cycle, it is necessary to produce a load of wafers through to the first deglaze. The lot is then split and the wafers are put through incremental LTO cycles after which they are checked by one of several methods to determine the required LTO cycle.

A common method to determine the LTO cycle is to measure incremental percent changes in sheet resistance after the deglaze after LTO step. A “knee” in percent change vs. LTO time curve (Figure 5) will correspond to the time required to remove the Si-B phase. It is desirable to oxidize 50-100 angstroms beyond the Si-B phase as this traps the defects in the oxide. Other methods for discerning the LTO cycle, such as deglazing and Sirtl or Wright etching to determine defect density and incremental oxide growth measurements, can be used. This step, kept during production, is used during process characterization and development. If the deglaze step is omitted from production, the subsequent drive should be run in a pure O<sub>2</sub> environment to prevent the formation of un-etchable silicon compounds



These recommendations are to be used as a starting point for all Boron Nitride PDS Products.

Following these recommendations will:

- 1) Develop a defect free boron diffused layer
- 2) Standardize your boron diffusion process for technical assistance
- 3) Allow defect free subsequent thermal processing.

Please contact us if you have questions regarding any of the information presented here.



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